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Research Article

Modulation Doping and Reduced Hysteresis in Monochalcogenide InSe/GaS Heterostructure 2D Field-Effect Transistors

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Cite This: *ACS Appl. Mater. Interfaces* 2025, 17, 35723−35731

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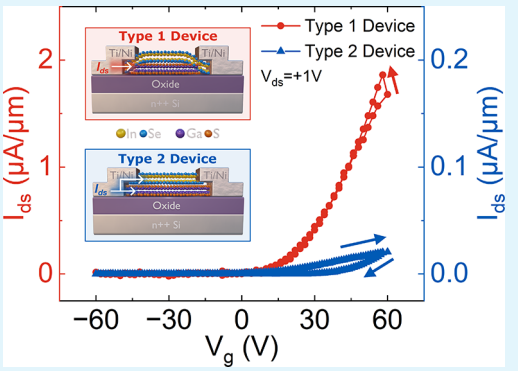
ABSTRACT: Heterostructures made from 2D materials have led to the discovery of many new electronic phases and have the potential for electronic devices with better performance. However, the mechanism by which charge is transferred or distributed in these novel heterostructure devices made of atomically thin semiconductors is yet to be fully understood. By creating and electronically characterizing InSe/GaS heterostructure field-effect transistors with different metal contact configurations, we observed a decrease in the maximum on-current and an increase in the hysteresis when both the InSe and GaS layers are in contact with the metal contacts. This, combined with the time-dependent conductance decay measurements, suggests that charge flow into the GaS from the metal contacts is the source of the hysteresis, which can be mitigated by encapsulating the GaS with InSe. Our resultant nearly hysteresis-free devices exhibit an average field-effect mobility of 34 ± 8 $cm^2V^{-1}s^{-1}$ at room temperature, comparable to that of bare InSe of the same size, with an average n-type modulation doping of ∼ 1 × 10^{12} cm^{-2} from the GaS layer.



KEYWORDS: *2D field-effect transistors, van der Waals heterostructures, modulation doping, hysteresis, threshold voltage, on-current, field-effect mobility, carrier density*

INTRODUCTION

Two-dimensional (2D) materials have garnered much interest in recent years due to their potential application in nano-[1−5] and opto-[6,7] electronics. Their novel physical properties,[8,9] the ease with which one can fabricate intricate device structures,[10−13] and the possibility of surpassing today's electronics' performance have made them a hot topic in academia.[14,15] Much attention has been paid to transition metal dichalcogenides, particularly MoS_2, and their possible use as channel materials in field-effect transistors (FETs). However, progress toward achieving high-performance MoS_2 FETs is limited by MoS_2's large effective mass, large density of point defects and charged impurities, and phonon scattering.[16−18]

Despite their promising properties, integration of 2D materials with conventional oxide dielectrics often results in poor device performance (e.g., low or average mobility,[3,19,20] large hysteresis,[21−23] low on/off ratio, large subthreshold swing[12,24,25]). These effects have been attributed to the large density of scattering centers present at the semiconductor/dielectric interface, such as Coulomb impurities, charge traps, and defects, mainly from the oxide layer.[26,27] These results highlight the role of the semiconductor-dielectric interface quality on the performance of FETs.

In an attempt to mitigate this issue, different insulators have been used, from polymer-based[28] to high-κ dielectrics, to try to improve the interface quality and increase electrostatic control. However, polymer-based dielectrics are limited by the maximum temperature they can withstand, and high-κ dielectrics have been observed to increase surface optical phonon scattering. Recently, the potential of 2D materials as dielectrics has been realized[29] in the form of 2D heterostructures. The lack of dangling bonds at the interface of these 2D heterostructures, as well as their small lattice mismatch, reduces possible scattering sources, resulting in better device performance. Additionally, these 2D dielectrics have the potential to tune the electronic properties of their neighboring layer, through either interfacial charge transfer[30] or proximity effects. Efforts toward the high-quality epitaxial growth of these heterostructures have been realized for particular 2D heterostructures such as Janus MoSSe[31] and WSe_2−MoS_2 lateral p−n junctions.[32]

GaS, a group III−VI monochalcogenide (MX, M = Ga, In; X = S, Se, Te), is a wide-bandgap semiconductor (E_g = 2−3.05

Received: March 4, 2025
Revised: May 5, 2025
Accepted: May 26, 2025
Published: June 6, 2025

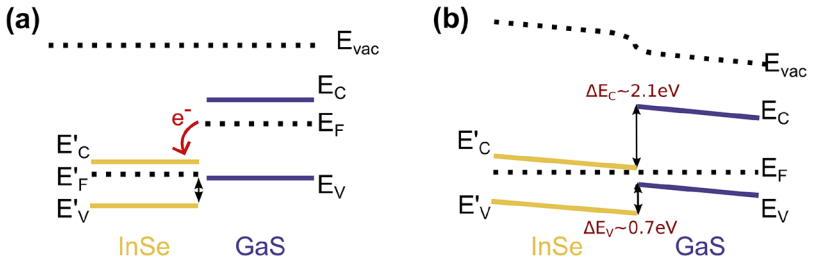


Figure 1. Band alignment of InSe and GaS (a) before and (b) after contact.

eV for decreasing thickness) mainly studied for its uses in optoelectronics.[33−37] Recently, the potential of GaS as a dielectric was proven by Shin et al.,[38] with their GaS/MoS_2 top-gated heterostructures exhibiting low subthreshold swing and better mobility than bare MoS_2. However, as aforementioned, MoS_2's large effective mass makes it less appealing for high-performance FETs. InSe, a fellow layered semiconductor, with an effective mass four times smaller than that of MoS_2, has already been shown to possess a mobility of 1000 $cm^2V^{-1}s^{-1}$ at room temperature,[26] making it a better candidate for an active channel material.

In this paper, we explore the role of metal contact with GaS on the device performance of InSe/GaS heterostructures. When joined together, these semiconductors form a type II staggered band alignment (Figure 1).[39−42] Because the Fermi level of GaS lies slightly higher than that of InSe, electrons will flow from GaS to InSe until equilibrium is reached (Figure 1b). This accumulation of carriers in InSe, as well as the cleaner interface provided by the absence of dangling bonds and small lattice mismatch, should in theory lead to a higher field-effect mobility. However, we find that this is only the case when the heterostructures are aligned such that the GaS is fully encapsulated by the InSe, indicating that metal contact connecting both InSe and GaS facilitates charge transfer from InSe to GaS. At a large gate voltage (>20 V), this leads to major electron trapping at the interface, which leads to decreased current in the InSe layer and larger hysteresis.

EXPERIMENTAL SECTION

GaS flakes were exfoliated from a bulk crystal by the standard Scotch tape method onto a clean, highly doped Si substrate with a 300 nm SiO_2 capping layer. Samples were then annealed for 1 h at 200 °C under vacuum to remove any tape residue. To form the various heterostructures presented in this paper, a polydimethylsiloxane stamp on a glass slide was used to pick up exfoliated InSe nanoflakes and then stacked on top of the desired GaS flake. InSe flakes were selected to be either larger or smaller in area than the GaS flake. Hereinafter, devices with GaS fully encapsulated by InSe will be referred to as type 1 devices, and devices with GaS not fully covered by the InSe and touching the metal pads will be referred to as type 2 devices. A third device structure, with the InSe/GaS heterostructure contacted by one pad and bare InSe contacting the other pad, was also made to explore the effect of metal contact on the GaS on the performance of our FETs. However, we will not include this device in our main discussion. A total of at least eight devices were created for each device type, and hereafter, when stating a device metric, it is assumed that it is taken to be the average taken from these devices. The transfer curves and device metrics can be found in Sections S3 and S4, Figures S5b and S6b.

To define metal contacts, a copper grid was used as a shadow mask, and e-beam evaporation was used to deposit 30 nm of titanium (Ti) and 60 nm of nickel (Ni). The resulting heterostructures were then annealed again under the aforementioned conditions to improve the InSe/GaS and Ti/heterostructure interface.

A micro-Raman scattering experiment was conducted at room temperature using a Horiba Jobin Yvon LabRam HR800 spectrometer equipped with a carrier coupled device detector and two grating systems (600 and 1800 lines/mm). A He−Ne laser (λ = 632.8 nm) was used with an Olympus optical microscope, BH-2. The laser power used was 17 mW with a spot size of 1 μm^2. The calibration of the Raman shift was done by using the 520 cm^{-1} line of a silicon wafer. The laser was focused on the channel area to verify the phase of our flakes and ensure the quality of the resulting heterostructures was intact after processing.

Electrical measurements were performed at room temperature in a Lakeshore probe station using a custom Labview program for data collection. Output curves sweeping the source-drain voltage from ±1 V were used to characterize the contact behavior (as Ohmic or Schottky) at zero and nonzero gate voltages. Additionally, transfer curves at various gate voltage ranges (±20, ±40, ±60 V) were used to explore the hysteretic behavior of our heterostructures. The source-drain current was normalized by the width of the transistor to display the current density. This was done to ensure a fairer comparison between devices of different geometries.

The threshold voltage, V_T, defined as the gate voltage needed to turn the device on, is extracted from transfer curves by performing a regression fit in the linear regime of the transfer curves and finding the value of V_g when I_{ds} is zero.[43] The field-effect mobility, μ, is also calculated from the transfer curves by extracting the transconductance, $g = (dI_{ds}/dV_g)|_{V_{ds}}$, in the linear regime[44] and plugging it into the expression

$$\mu = \frac{L}{W}\frac{g}{C_{ox}V_{ds}} \quad (1)$$

where L is the channel length, W is the channel width, C_{ox} is the oxide capacitance (1.1 nF/cm^2 for 300 nm SiO_2), and V_{ds} is the source-drain voltage. It quantifies how easily carriers move in the channel under the application of a gate voltage and provides information about the scattering centers in the channel.

Time-dependent conductance measurements were performed to investigate and compare the time relaxation effects in both types of devices. Low-temperature measurements were conducted on bare InSe and its heterostructures to confirm modulation doping from the GaS layer to the InSe layer. Finally, atomic force microscopy scans were obtained with an Agilent MAC Mode III atomic force microscope using a 4 μm wide Bruker TESPD antimony doped silicon tip. Scans were taken in a direction parallel to the channel at a speed of 256 points per line and 0.1 lines per second. Height profiles were obtained along the channel area to obtain thickness measurements of our flakes (Figures S1 and S2).

RESULTS AND DISCUSSION

The Raman spectra for our bare InSe and GaS devices as well as their heterostructures can be found in Figure 3. The laser was focused on the channel area of each device, making sure that it overlapped the heterostructure. For γ-InSe, four Raman modes are expected:[45] A^1_{1g}, E^1_{2g}, A^1_{1g}(LO), and A^2_{1g}. However, because of the wavelength of our laser, we were able to probe wavenumbers larger than 200 cm^{-1} and thus detect only the

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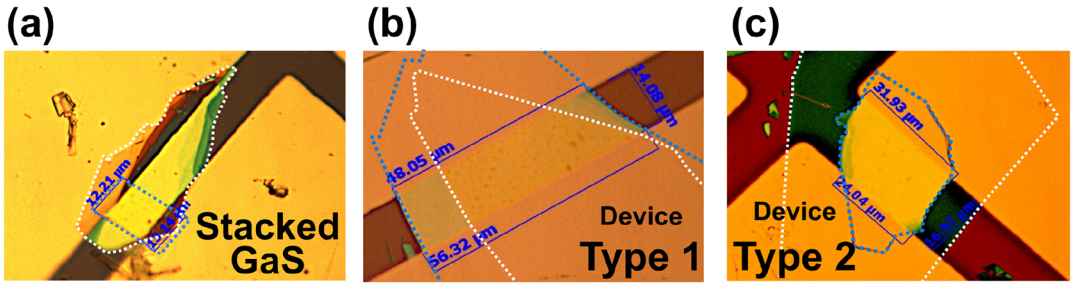

Figure 2. Optical images of (a) the premade InSe transistor with GaS stacked on top of it, (b) an example of a type 1 device, and (c) an example of a type 2 device. The blue dotted line marks the InSe flake, and the white dotted line marks the GaS flake in these images.

last mode. Our bare InSe devices display the characteristic A^2_{1g} mode at 226 cm^{-1}, and the peak remains for the two device types presented in this paper.

Bulk β-GaS has peaks at 187, 289, and 368 cm^{-1} corresponding to the A^1_{1g}, E^1_{2g}, and A^2_{1g} modes.[46] Our bare GaS display peaks at 302 and 359 cm^{-1}, blue-shifted and red-shifted compared to the E^1_{2g} and A^2_{1g} modes, respectively, which is expected as GaS is peeled to thinner layers.[46−48] These peaks are still detectable in the heterostructures; thus, we can conclude that no major structural changes come about when InSe is placed on top of GaS.

A multilayer GaS flake was stacked on top of a premade InSe transistor (Figures 2a and 4a) to investigate its effect on InSe.

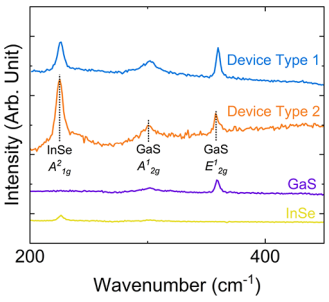

Figure 3. Raman spectra of type 1 and type 2 devices as well as bare GaS and InSe FETs.

The transfer curve of this device before and after the GaS stacking (Figure 4b) shows a clear shift in threshold voltage to the left, indicative of the electron transfer from the GaS to the InSe layer. This is seen across multiple devices, with the average threshold voltage decreasing from 20 ± 1 to 10 ± 2 V upon stacking of GaS on the premade InSe device. The increase in the field-effect mobility from 90 ± 10 to 100 ± 20 $cm^2V^{-1}s^{-1}$ after GaS stacking is within the standard deviation of the bare InSe mobility, suggesting the increase in mobility to be a minor effect. Multiple premade InSe devices were stacked with GaS flakes, and the change in their mobility (Figure 4c) and threshold voltage shifts (Figure 4d) confirm our hypothesis on charge transfer from GaS to InSe and the relatively minor effect of GaS encapsulation on the InSe layer's mobility. The variance in the mobility and threshold voltage in our devices can be attributed to the variance in material thickness[33,49−53] and defect density[54] present in both InSe and GaS flakes.

Figure 5b,d shows the representative transfer curves for the two device types examined in this paper with the GaS layer underneath InSe. For this measurement, the gate voltage was swept from 0 to −60 V, back to 0 V, up to +60 V (up-sweep),

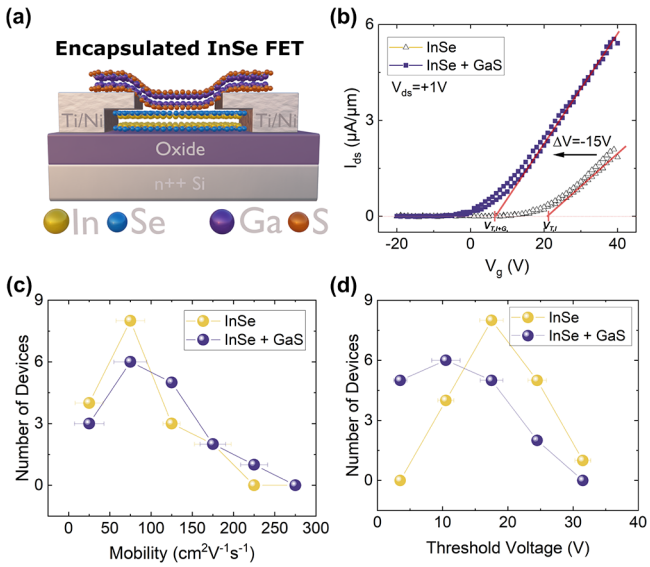

Figure 4. (a) Schematic cross-section view of a GaS-capped InSe FET. (b) Transfer curve of InSe FET before and after capping with GaS. Counts of (c) mobility and (d) threshold voltages of InSe FET before and after encapsulating with GaS.

and back again to 0 V (down-sweep) while a constant V_{ds} = +1 V was applied between the source and the drain. All devices exhibit clear n-type behavior, as expected for standalone InSe and GaS FETs (Figures S3 and S4), and a similar subthreshold swing to that of bare InSe (4−10 V/dec). However, the mobility, on-current, and degree of hysteresis are different for each device type.

The average mobilities of type 1 and 2 devices are 30 ± 8 and 20 ± 5 $cm^2V^{-1}s^{-1}$, respectively, much lower than the mobility of bare InSe and GaS-capped InSe FETs. Note that these values are smaller if only considering the up-sweep and larger if only considering the down-sweep. This suggests that the discharging of the InSe layer during the down-sweep is more efficient than the charging during the up-sweep. While both structures display larger hysteresis and smaller on-currents than the GaS-stacked InSe FETs, type 1 devices show a smaller average threshold voltage (14 ± 4 V) than bare InSe, similar to the GaS-stacked InSe FETs. We attribute the difference in mobility, hysteresis, and on-current between the GaS-capped InSe FET and type 1,2 devices to the lack of direct contact between the GaS layer and the oxide in the GaS-capped InSe FET.

As seen from Figure 6, type 1 device samples on average have higher on-currents (1.9 ± 0.4 μA/μm compared to 0.2 ± 0.1 μA/μm) and considerably smaller hysteresis than type 2

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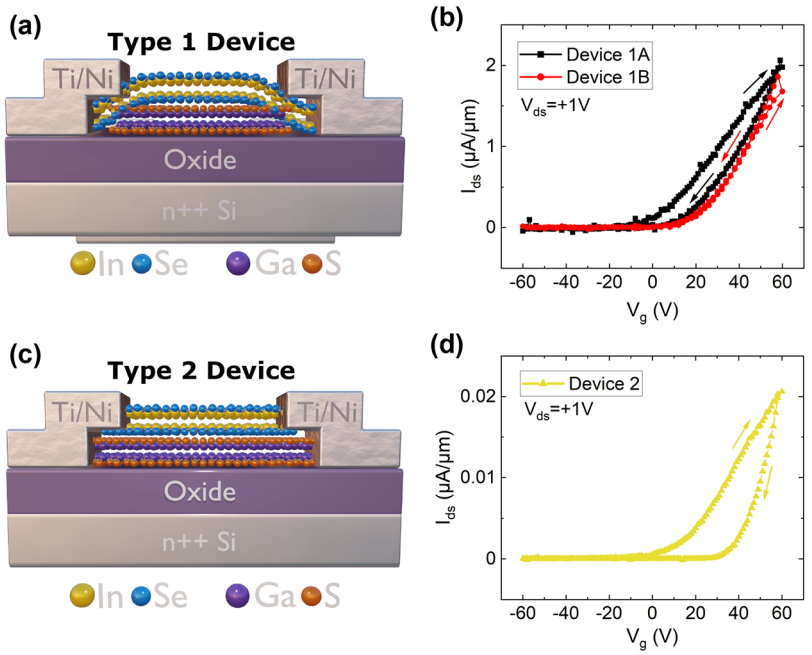

Figure 5. Cross section and transfer curve of the type 1 device (a, b) and the type 2 device (c, d).

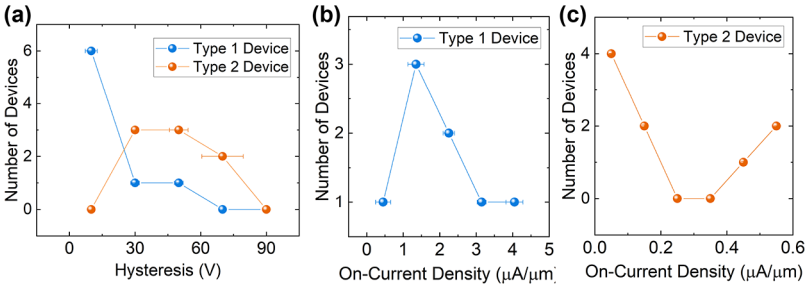

Figure 6. (a) Number of devices measured with a given hysteresis for type 1 and 2 devices. On-current distribution for type 1 (b) and type 2 (c) devices.

device samples (20 ± 6 V compared to 50 ± 6 V). Since the only difference between these two devices is whether the GaS is in contact with the metal, our results suggest that the hysteresis and the decrease in on-current and mobility are caused by current injection into the GaS layer through the metal contacts. Hysteresis is a common phenomenon in FETs made from 2D heterostructures,[55−57] but it is usually attributed to charge transfer and/or trapping induced by the application of a large gate voltage. In the case where the heterostructure consists of a 2D semiconductor and a large bandgap insulator (e.g., hBN), the charge trapping mainly occurs through electron tunneling.[58,59] When the heterostructure consists of a 2D semiconductor (InSe in our case) and another 2D semiconductor with a larger bandgap (GaS in our case), the drastic band bending of the wider bandgap semiconductor by the gate voltage can result in the formation of a triangular potential well at the interface between the wide-bandgap semiconductor (GaS) and the dielectric (SiO_2) on the substrate that acts as a charge trapping layer. A similar situation was discussed in our prior study of the InSe/GaSe interface, where the barrier of GaSe was lower and the hysteresis was more severe.[30] The presence of this extra current pathway splits the source−drain current into two and results in a decrease in on-current in type 2 devices. The charges flowing through the GaS can also be trapped within the layer, which exacerbates the hysteresis observed in type 2 devices. Moreover, it has been reported that direct contact between metal and semiconductor can induce surface phonons that decrease the mobility[34,60,61] and could explain the decrease in mobility of type 2 devices.

Though GaS and Ti make a Schottky contact with a potential barrier of about 2 eV, the thickness of the GaS flakes used in this paper is at most 10 nm, making the width of this triangular potential small enough that tunneling from the metal to the GaS can occur at sufficiently high gate voltages. This results in the range-dependent hysteresis: as the gate voltage is swept from 0 to $-V_g$, the electron trap states in GaS start to deplete, with more traps depleted if a more negative $V_{g,max}$ is swept (Figure 7c). These positively charged traps make the potential seen by the InSe more positive than the applied V_g, hence the turning on of the device at negative V_g. As V_g is swept to more positive V_g, the traps in GaS begin to charge up, offsetting some of the current flowing into the InSe layer. Note that when the GaS layer is not in direct contact with the metal contact (type 1 device), the charging/discharging speed of the GaS layer is much slower than the case where the charging/discharging can go through metal contacts (type 2 device). This results in the type 1 devices responding to the gate voltage change mainly through the InSe layer, behaving more like bare InSe FETs. For type 2 devices where the charging of

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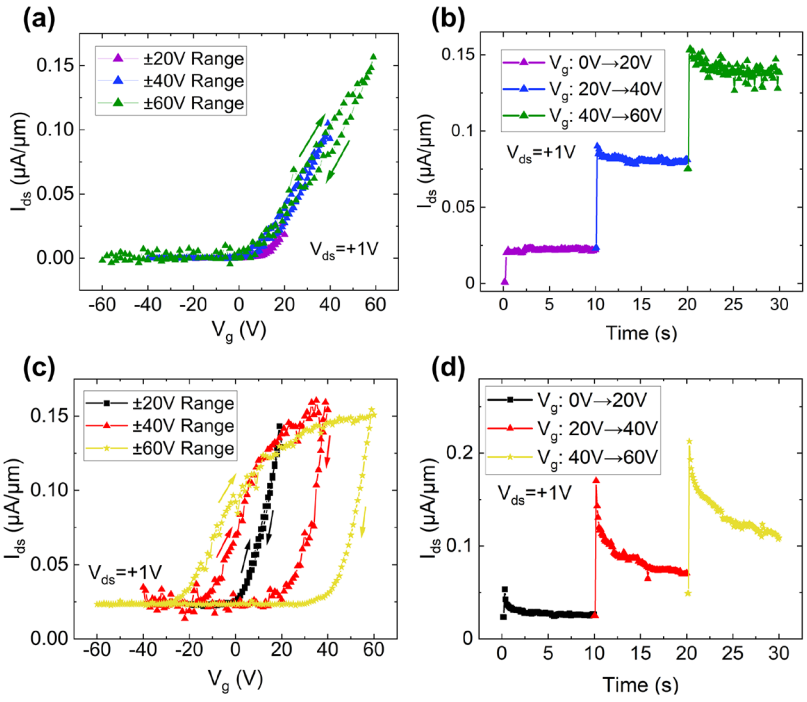

Figure 7. (a)/(c) Example transfer curves and (b)/(d) time-dependent conductance measurements of type 1 and type 2 devices.

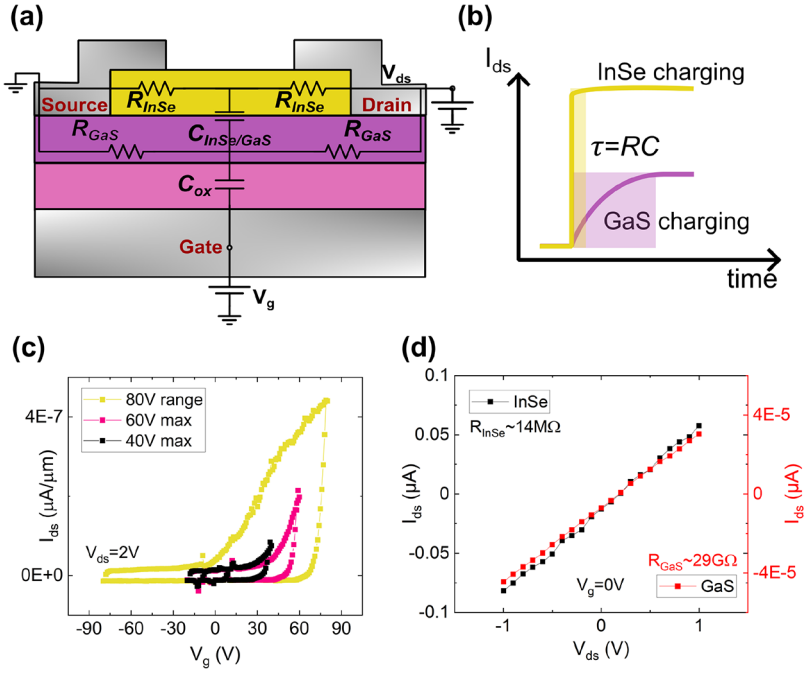

Figure 8. (a) Equivalent circuit for type 2 devices. (b) Illustrative source−drain current as a function of time for InSe (yellow) and GaS (purple) FETs upon sudden turning on the gate voltage. (c) Transfer curve of the bare GaS FET. (d) Current−voltage curve of the bare InSe (red) and GaS (black) FETs.

the GaS layer can go through the source/drain metal contacts, the time constant for the GaS layer's charging/discharging is still much longer than the InSe layer (see Figure 8 and related discussion), giving rise to the strong hysteresis in these devices.

To further test the role of the GaS layer on the electron flow through these heterostructures, time-dependent conductance measurements were taken for each device type. A constant source−drain voltage of +1 V was applied across the channel, while the gate voltage was increased from 0 to +60 V and back down to 0 V in 20 V increments. Type 1 devices stabilize very quickly (Figure 7b) at low gate voltages, as evident from the small time decay when going from 0 to 20 V, but experience a decay when biased to higher gate voltages. In contrast, type 2 devices exhibit a clear time relaxation effect even at low gate voltages (Figure 7d). Recall, type 2 devices have GaS making contact with the source and drain pads, whereas type 1 devices have GaS fully encapsulated by InSe, with the metal pads only contacting the InSe. As a result, the current in type 1 devices is

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limited to the InSe flake, while in type 2 devices, the current is divided between InSe and GaS flakes.

We can model this system as an RC circuit (Figure 8a), with the number of resistors determined by the number of semiconductors contacting the metal. For type 1 devices, the relaxation time, τ, is determined simply by the resistance of the InSe layer and the equivalent capacitance of the circuit, $C_{eq} = (C_{InSe/GaS}^{-1} + C_{ox}^{-1})^{-1}$, which is dominated by the capacitance of the SiO_2 since the InSe and GaS layers are much thinner. Taking the average resistance of ungated InSe, $R = 14$ MΩ, the equivalent capacitance $C_{eq} = 11$ nF/cm^2, and the area of the InSe flake to be $A_{InSe} = 2.8 \times 10^{-5}$ cm^2, the resultant time constant for InSe is $\tau_{InSe} = 4$ μs. In other words, InSe charges and discharges very quickly (Figure 8b).

In contrast, contact with GaS in type 2 devices leads to an additional resistor in the circuit that provides the current with an extra pathway to flow. This resistor, R_{GaS}, is several orders of magnitude larger than R_{InSe} (Figure 8d), especially at higher gate voltages (Figure 8c), and connects the contacts to the equivalent capacitor created by the InSe and GaS layers, $C_{InSe/GaS}$. The resistance of the GaS layer can be taken from output curves (red curve in Figure 8d), with $R_{GaS} = 29$ GΩ. The capacitance of the InSe and GaS layers can be calculated using the formula for a parallel capacitor with a dielectric constant of $\epsilon = 8$ and using the average thickness of type 2 devices, $d_{InSe} = 30$ nm and $d_{GaS} = 10$ nm, respectively, and we obtain $C_{InSe/GaS} = (C_{InSe}^{-1} + C_{GaS}^{-1})^{-1} = 10^3$ nF/cm^2. Thus, the RC time constant for the GaS and InSe bilayer is $\tau_{InSe/GaS} \approx 0.8$ s, which is closer in magnitude to the discharge time that we obtained in our time-dependent conductance measurements. This current splitting between the GaS and InSe layers explains the increase in hysteresis and smaller on-current for type 2 devices. In GaS-capped InSe FETs, the lack of connection between GaS and $C_{InSe/GaS}$ leads the channel to have a relaxation time of bare InSe, and hence the smaller hysteresis and larger on-current in these devices.

To investigate the mobility of our heterostructure devices and bare InSe FETs, we obtain transfer curves at temperatures ranging from 77 to 320 K (Figures S7 and S8). A plot of the extracted mobility as a function of temperature is present in Figure 9. The half-filled symbols connected with dotted lines in Figure 9 represent the bare InSe FETs, while the filled symbols connected by a solid line represent the type 1 device heterostructures. The variation in mobility from device to device can be attributed to variations in the InSe film thickness. The InSe thicknesses in devices i8, i9, i10, and i49 are 11, 50, 20, and 14 nm (Figure S1). The room-temperature mobility seems to increase as the thickness increases from 11 to 50 nm, consistent with previous InSe transistors on SiO_2.[62] This increase in mobility with increasing thickness has been attributed to the screening of charge traps at the semiconductor/oxide interface.[63−65]

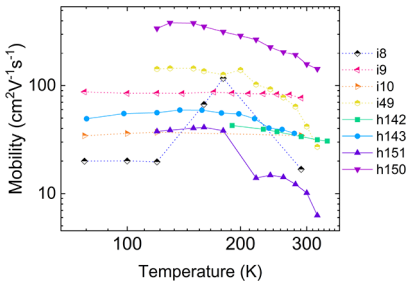

Figure 9. Plot of mobility as a function of temperature for our type 1 devices and bare InSe FETs. The half-filled symbols connected with dotted lines represent the bare InSe devices, while the filled symbols connected with a solid line represent our type 1 devices.

The relationship between flake thickness and mobility is not as trivial in our heterostructured devices because of the variance in both InSe and GaS thickness. Nonetheless, we observe an increase in the room-temperature mobility with a decreasing GaS thickness. The device with the highest room-temperature mobility is h151, with InSe and GaS thicknesses of 20 and 10 nm, respectively. Meanwhile, the device with the lowest room-temperature mobility is h150, which has InSe and GaS thicknesses of 37 and 16 nm, respectively. Since we know from our study of bare InSe FETs that the mobility of InSe increases with layer thickness, we can conclude that the decrease in mobility in our heterostructure devices originates from the increasing thickness in the GaS layer. This phenomenon has also been reported in AlGaN/GaN heterostructures, where the increase in AlGaN thickness resulted in an increase of the mobility up to a certain AlGaN thickness, after which it declined.[66] This is attributed to a decrease in the barrier height between the two heterostructures[67] as well as the increase in alloy disorder and interface roughness scattering[68,69] with increasing AlGaN thickness. Similar conclusions can be drawn with our InSe/GaS heterostructures. With increasing thickness, the bandgap of GaS decreases and thus so does the conduction band edge difference between it and InSe. This can result in a smaller barrier height at the interface, which can allow electron states in the GaS layer to penetrate into the InSe. Additionally, the increase in defect states in thicker GaS flakes can also lead to a decrease in mobility with increasing GaS thickness.

The mobility of FETs is affected by different scattering mechanisms in different temperature regimes. At low T, charge impurity scattering and acoustic phonon scattering are the dominant scattering mechanisms. They manifest themselves with a positive power law dependence of the form $\mu \propto T^{\gamma}$, where $\gamma = +1.5$. Conversely, at high T, the mobility is limited by optical phonon scattering, where $\gamma = -1.5$. As a result, the log-plot of mobility as a function of temperature has a positive slope for low T and a negative slope for high T. However, both our bare and heterostructure devices deviate from these theoretical values.[70] Our thinner InSe flakes (i8 and i49) display a larger temperature dependence than the thicker flakes (i10 and i9), particularly at temperatures above 180 K, potentially due to the increased effect of optical phonons that the thinner flakes are not able to screen. By taking the linear fit from the peak of the graph ($T = 180$ K) to our highest temperature ($T = 320$ K), we obtain γ values of −4.1 and −3.2 for i8 and i49, respectively. This value is an order of magnitude smaller in our thicker InSe samples, $\gamma = -0.1$, signaling the larger impact of phonon scattering in thinner samples than in thicker ones. A similar trend is present in our heterostructures, where γ ranges from −1 to 2.5, with the smallest value coming from the device with thicker GaS and InSe flakes.

When examining the carrier density of our devices, we note a larger average current density in our heterostructures than in bare InSe FETs, even at low temperatures, signifying doping in InSe from the GaS layer. Threshold voltages for four bare InSe devices and four type 1 device samples were obtained at different temperatures, from 77 to 320 K, and used to calculate their carrier density. Taking the carrier density to be $n = C_{ox}(V_g$

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$- V_{Th}$), where C_{ox} is the capacitance of the silicon oxide (1.15 μF/cm^2 for 300 nm SiO_2), V_g is the applied gate voltage, and V_{Th} is the threshold voltage of the device, we plot it against temperature at V_g = 50 V to obtain Figure 10. The average carrier density of type 1 devices is well above 10^{12} cm^{-2} and does not drop drastically at high temperatures, indicative of a doping of approximately 1×10^{12} cm^{-2}.

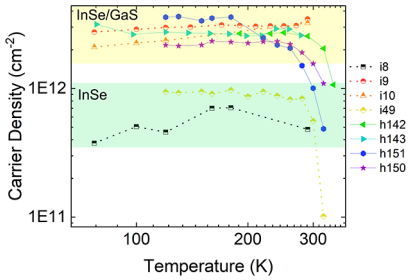

Figure 10. Carrier density for type 1 device samples and bare InSe devices as a function of temperature.

In contrast, the carrier density of bare InSe ranges from 4×10^{12} to 3×10^{11} cm^{-2}. This spread in carrier density can be attributed to the varying thicknesses of the InSe flakes measured, with the higher carrier density corresponding to the thicker InSe flake (50 nm) and the lowest carrier density being that of the thinnest InSe flake (11 nm). Type 1 devices, on the other hand, tend to have a carrier density much higher than that of the thin InSe transistors, regardless of InSe and GaS thickness. This can be used to increase the carrier concentration in thinner InSe samples, which we know suffer from low electron concentrations (i8 and i49 in Figure 10), to achieve doping concentrations closer to what is obtainable in thicker InSe flakes, with the additional benefit of decreasing charge scattering at low T.

CONCLUSIONS

In this paper, we have studied the electron transport properties of InSe/GaS heterostructures, wherein GaS is fully encapsulated by InSe (type 1 device) and GaS is contacting both pads (type 2 device). We have found that out of both devices, type 1 devices display the smallest hysteresis with the largest on-current and mobility. We attribute the lower performance of the type 2 device to current splitting between the InSe and GaS layers both making contact with the metal pads and its slow time constant. Additionally, we have shown the potential of GaS to modulate the carrier density of InSe and increase the mobility at low temperatures. This study can aid in the design and understanding of future 2D heterostructures with the desired electronic properties.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.5c04399.

AFM height profiles for thickness determination; bare InSe and GaS FET transfer characteristics; transfer characteristics and device metrics for type1 devices; transfer characteristics and device metrics for type2 devices; temperature-dependent transfer curves for bareInSe and type 1 devices; and additional supporting figures and tables (PDF)

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

X.P.A.G. acknowledges the support from NSF (DMR-1607631) and a generous grant from the Expanding Horizons Initiative (EHI), College of Arts and Sciences, Case Western Reserve University. R.S. acknowledges the financial support provided by the Ministry of Science and Technology in Taiwan under Project No. NSTC (113-2124-M-001-045-MY3 and 113-2124-M-001-003), financial support from the Center of Atomic Initiative for New Materials (AI-Mat), National Taiwan University (Project No. 113L900801), and Academia Sinica for the budget of AS-iMATE-113-12.

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